

IN74HC05A

Hex Inverter with Open-Drain Outputs

The IN74HC05A is identical in pinout to the LS/ALS05. The device inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LS/ALS TTL outputs.

This device contains six independent gates, each of which performs the logic INVERT function. The open-drain outputs require external pull-up resistors for proper logical operation. They may be connected to other open-drain outputs to implement active-high wired-AND functions.

- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 2.0 to 6.0 V
- Low Input Current: 1.0 μ A
- High Noise Immunity Characteristic of CMOS Devices

N SUFFIX PLASTIC

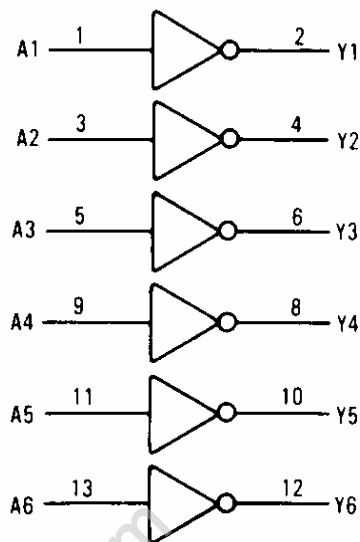
D SUFFIX SOIC

ORDERING INFORMATION

IN74HC05AN Plastic
IN74HC05AD SOIC

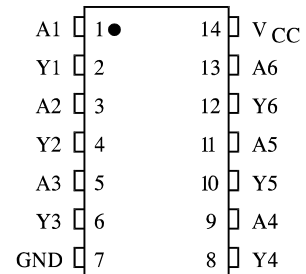
$T_A = -55^\circ$ to 125° C for all packages

LOGIC DIAGRAM



PIN 14 = V_{CC}
PIN 7 = GND

PIN ASSIGNMENT



FUNCTION TABLE

Inputs	Output
A	Y
L	Z
H	L

Z = High Impedance

MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V _{CC}	DC Supply Voltage (Referenced to GND)	-0.5 to +7.0	V
V _{IN}	DC Input Voltage (Referenced to GND)	-1.5 to V _{CC} +1.5	V
V _{OUT}	DC Output Voltage (Referenced to GND)	-0.5 to V _{CC} +0.5	V
I _{IN}	DC Input Current, per Pin	±20	mA
I _{OUT}	DC Output Current, per Pin	±25	mA
I _{CC}	DC Supply Current, V _{CC} and GND Pins	±50	mA
P _D	Power Dissipation in Still Air, Plastic DIP** SOIC Package**	750 500	mW
T _{stg}	Storage Temperature	-65 to +150	°C
T _L	Lead Temperature, 1 mm from Case for 10 Seconds (Plastic DIP or SOIC Package)	260	°C

*Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the Recommended Operating Conditions.

**Derating - Plastic DIP: - 10 mW/°C from 65° to 125°C
SOIC Package: - 7 mW/°C from 65° to 125°C

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
V _{CC}	DC Supply Voltage (Referenced to GND)	2.0	6.0	V
V _{IN} , V _{OUT}	DC Input Voltage, Output Voltage (Referenced to GND)	0	V _{CC}	V
T _A	Operating Temperature, All Package Types	-55	+125	°C
t _r , t _f	Input Rise and Fall Time (Figure 1)			
	V _{CC} =2.0 V	0	1000	ns
	V _{CC} =4.5 V	0	500	
	V _{CC} =6.0 V	0	400	

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{IN} and V_{OUT} should be constrained to the range GND ≤ (V_{IN} or V_{OUT}) ≤ V_{CC}.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). Unused outputs must be left open.

DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

Symbol	Parameter	Test Conditions	V _{CC} V	Guaranteed Limit			Unit
				25 °C to -55°C	≤85 °C	≤125 °C	
V _{IL}	Low -Level Input Voltage	V _{OUT} = V _{CC} or 0 V I _{OUT} ≤ ±0.5 μA (T= -55 to 25°C) I _{OUT} ≤ ±5.0 μA (T= 85°C) I _{OUT} ≤ ±10 μA (T= 125°C)	2.0	0.5	0.5	0.5	V
			4.5	1.35	1.35	1.35	
			6.0	1.8	1.8	1.8	
V _{IH}	High-Level Input Voltage	V _{OUT} ≤ 0.1 V I _{OUT} ≤ 20 μA	2.0	1.5	1.5	1.5	V
			4.5	3.15	3.15	3.15	
			6.0	4.2	4.2	4.2	
V _{OL}	Low - Level Output Voltage	V _{IN} =V _{IH} I _{OUT} ≤ 20 μA	2.0	0.1	0.1	0.1	V
			4.5	0.1	0.1	0.1	
			6.0	0.1	0.1	0.1	
		V _{IN} =V _{IH} I _{OUT} ≤ 4.0 mA	4.5	0.26	0.33	0.4	
			6.0	0.26	0.33	0.40	
			6.0	0.26	0.33	0.40	
I _{IL}	Input Leakage Current	V _{IL} = GND	6.0	-0.1	-1.0	-1.0	μA
I _{IH}	Input Leakage Current	V _{IH} =V _{CC}	6.0	-0.1	-1.0	-1.0	μA
I _{CC}	Quiescent Supply Current (per Package)	V _{IL} =GND V _{IH} =V _{CC} I _{OUT} =0 μA	6.0	1.0	10	40	μA
I _{OZL}	Three-State Leakage Current	V _{IN} = V _{IL} or V _{IH} V _{OUT} = GND	6.0	-0.5	-5.0	-10	μA
I _{OZH}	Three-State Leakage Current	V _{IN} = V _{IL} or V _{IH} V _{OUT} = V _{CC}	6.0	-0.5	-5.0	-10	μA

AC ELECTRICAL CHARACTERISTICS ($C_L=50\text{pF}$, Input $t_r=t_f=6.0\text{ ns}$)

Symbol	Parameter	Test Conditions	V _{CC} V	Guaranteed Limit			Unit
				25 °C to -55°C	≤85 °C	≤125 °C	
t _{PLZ} , t _{PZL}	Propagation Delay, Input A to Output Y (Figures 1 and 2)	V _{IL} = GND V _{IH} = V _{CC} t _{LH} = t _{HL} = 6 ns C _L = 50 pF	2.0	120	150	180	ns
			4.5	24	30	36	
			6.0	20	26	31	
t _{THL}	Output Transition Time, Any Output (Figures 1 and 2)	V _{IL} = GND V _{IH} = V _{CC} t _{LH} = t _{HL} = 6 ns C _L = 50 pF	2.0	75	95	110	ns
			4.5	15	19	22	
			6.0	13	16	19	
C _{IN}	Input Capacitance			10	10	10	pF
C _{OUT}	Three-State Output Capacitance (Output in High- Impedance State)			10	10	10	pF

C _{PD}	Power Dissipation Capacitance (Per Gate)	Typical @25°C, V _{CC} =5.0 V	pF
	Used to determine the no-load dynamic power consumption: $P_D=C_{PD}V_{CC}^2f+I_{CC}V_{CC}$	8.0	

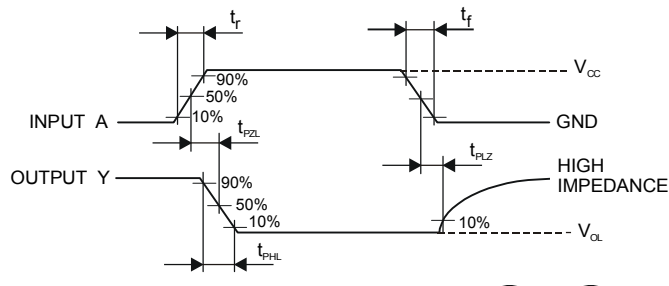


Figure 1. Switching Waveforms

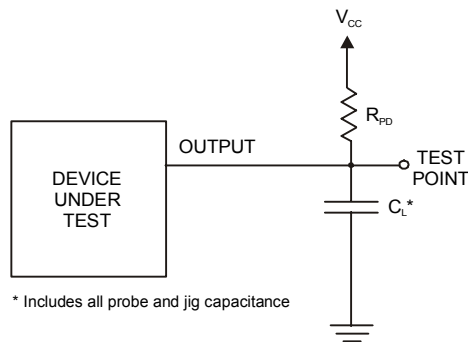


Figure 2. Test Circuit

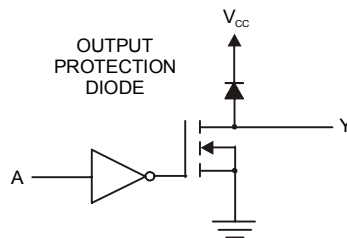
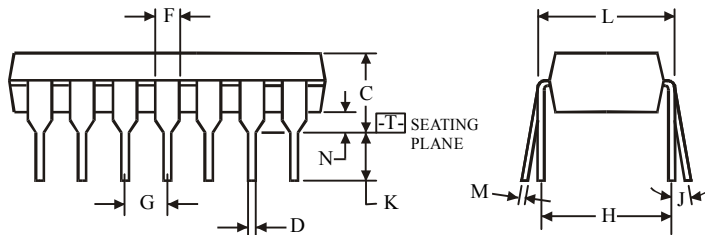
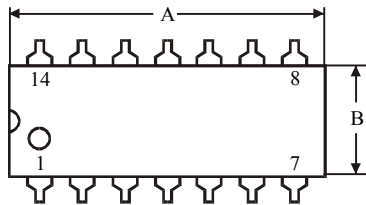
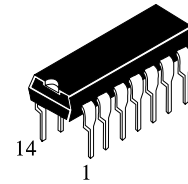


Figure 3. Expanded Logic Diagram (1/6 of the Device)

**N SUFFIX PLASTIC DIP
(MS - 001AA)**



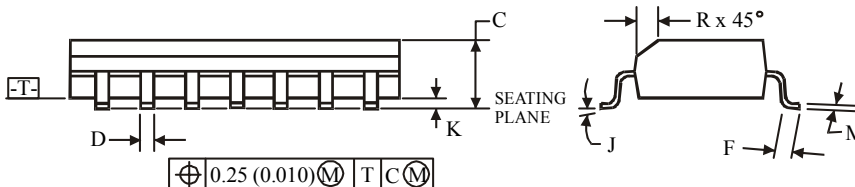
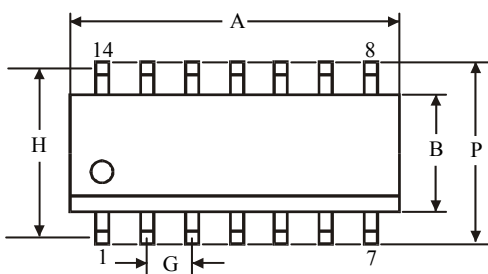
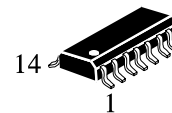
$\oplus 0.25 (0.010) \text{ (M) T}$

NOTES:

- Dimensions "A", "B" do not include mold flash or protrusions.
Maximum mold flash or protrusions 0.25 mm (0.010) per side.

Symbol	Dimension, mm	
	MIN	MAX
A	18.67	19.69
B	6.1	7.11
C		5.33
D	0.36	0.56
F	1.14	1.78
G	2.54	
H	7.62	
J	0°	10°
K	2.92	3.81
L	7.62	8.26
M	0.2	0.36
N	0.38	

**D SUFFIX SOIC
(MS - 012AB)**



$\oplus 0.25 (0.010) \text{ (M) T C (M)}$

NOTES:

- Dimensions A and B do not include mold flash or protrusion.
- Maximum mold flash or protrusion 0.15 mm (0.006) per side for A; for B - 0.25 mm (0.010) per side.

Symbol	Dimension, mm	
	MIN	MAX
A	8.55	8.75
B	3.8	4
C	1.35	1.75
D	0.33	0.51
F	0.4	1.27
G	1.27	
H	5.27	
J	0°	8°
K	0.1	0.25
M	0.19	0.25
P	5.8	6.2
R	0.25	0.5